3. (original): The multiplexing video decoding method of claim 1, wherein the decoding step further comprises:

incrementing an index value for a register corresponding to one of the plurality of channels to obtain information for a current channel when a decoding switching function is called;

determining whether decoding of the current channel corresponding to the index value is video-enabled; and

executing the decoding process if the current channel is video-enabled, and otherwise, switching to a decoding process of a next channel.

4. (original): The multiplexing video decoding method of claim 1, wherein video parameters and a program status to be decoded in each channel are designated whenever the decoding is switched from one of said plurality of channels to another of said plurality of channels.

5. (original): The multiplexing video decoding method of claim 1, further comprising a step for switching a task inside a waiting loop related to the decoding and display time control.

6. (original): A task switching method for switching channels to be decoded in signals of a plurality of channels in a multiplexing video decoding method, the task switching method comprising the steps of:

incrementing an index register value for a register corresponding to one of the plurality of channels to obtain information for a current channel when a task switching function is called;

finishing task switching if video decoding of the current channel corresponding to the index value is enabled, and otherwise, incrementing the index register value, and then switching to a next task, by obtaining a program state corresponding to a program counter value associated with a respective one of the plurality of channels.

7. (original): A multiplexing video decoding apparatus for receiving bit streams, each of said bit streams comprising a plurality of slices and received in a plurality of channels, and for decoding the bit stream of each of the plurality of channels, the multiplexing video decoding apparatus comprising:

a plurality of First-In First-Out (FIFO) units for transmitting in a first-in-first-out manner the bit streams of the plurality of channels in parallel;

a syntax processor for cyclically decoding the bit streams of the plurality of channels output from the plurality of FIFO units at a slice interval, by obtaining a program state corresponding to a program counter value associated with a respective one of the plurality of channels; and

a video processor for reproducing the bit stream of a corresponding channel decoded by the syntax processor into video data according to a predetermined video reproduction format.

8. (original): A multiplexing video decoding apparatus for receiving bit streams, each of said bit streams comprising a plurality of slices and received in a plurality of channels, and for decoding the bit stream of each of the plurality of channels, the multiplexing video decoding apparatus comprising:

a plurality of First-In First-Out (FIFO) units for transmitting in a first-in-first-out manner the bit streams of the plurality of channels in parallel;

a syntax processor for cyclically decoding the bit streams of the plurality of channels output from the plurality of FIFO units at a slice interval; and

a video processor for reproducing the bit stream of a corresponding channel decoded by the syntax processor into video data according to a predetermined video reproduction format, wherein the syntax processor comprises:

a plurality of stacks, each of said plurality of stacks respectively storing a program counter value of a channel to be decoded;

an index register for generating an index value for selecting a channel to be decoded from the plurality of stacks; and

a processor for selecting a channel to be decoded by slice by cyclically incrementing the index value of the index register and to obtain a program state corresponding to the program counter value that has been pushed into the respective one of the plurality of stacks for the channel.

9. (original): The multiplexing video decoding apparatus of claim 8, wherein the syntax processor switches a decoding task immediately after decoding a slice unit.

10. (original): The multiplexing video decoding apparatus of claim 9, further comprising a plurality of registers which independently store control parameters and program parameters of each channel bit stream and are designated in a multiplexed index register value mode.

11. (original): The multiplexing video decoding apparatus according to claim 8, wherein the syntax processor further includes a macroblock decoder to extract bit stream size and command information for a channel.

12. (original): The multiplexing video decoding apparatus according to claim 11, wherein the syntax processor further includes a bit stream decoder receiving said bit stream size and command information from said macroblock decoder to provide a reproduced bit stream for use by said video processor.

13. (original): The multiplexing video decoding apparatus of claim 8, wherein said index register further generates an index value for selecting one of said plurality of FIFCO units to obtain video bit steam information.

14. (new): The multiplexing video decoding apparatus of claim 7, wherein the syntax processor comprises:

a plurality of stacks, each of said plurality of stacks respectively storing the program counter value of a channel to be decoded;

an index register for generating an index value for selecting the channel to be decoded from the plurality of stacks; and

a processor for selecting the channel to be decoded by slice by cyclically incrementing the index value of the index register and to obtain the program state corresponding the program counter value that has been pushed into the respective one of the plurality of stacks for the channel.